CHIPS JOINT UNDERTAKING

Working together to strengthen European industries

Anton Chichkov,
Chips JU Head of Programmes and Communications

10 Mar 2026

FUNDING ECS INNOVATION IN EUROPE

September 2023

1. Strengthen Europe's research and technology leadership towards smaller and faster chips

2. Build and reinforce capacity to innovate in the design, manufacturing and packaging of advanced chips

...

4. Address the skills shortage, attract new talent and support the emergence of a skilled workforce

KDT JU
KEY DIGITAL TECHNOLOGIES JOINT UNDERTAKING

Chips JU

ECSEL JU

eniac JOINT UNDERTAKING

ARTEMIS

Nanoelectronics:
2.86 B€ costs

Embedded Systems
1.34 B€ costs

Electronic Comp & Systems:
4.69 B€ costs

Electronic Comp & Systems:
1.3 B€ EU funding

Chips for Europe Initiative:
2.8 B€ EU funding

2008 2014 2021 2023 2028

Chips JU

A One-Of-a-Kind Partnership for EU Chips Industry

Chips JU

TRI-PARTITE STRUCTURE

~ € 11 Bn

European Union	Participating States	Private Members
€ 4.175 Bn	€ 4.175 Bn	€ 2.500 Bn

A ONE-OF-A-KIND PARTNERSHIP FOR EUROPE'S CHIPS INDUSTRY

TRI-PARTITE REPRESENTATION

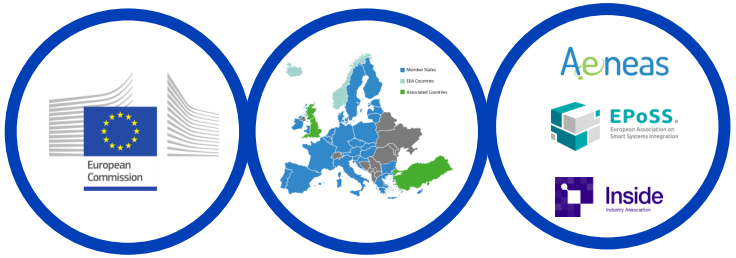
European Union
European Commission

Participating States
Public Authorities

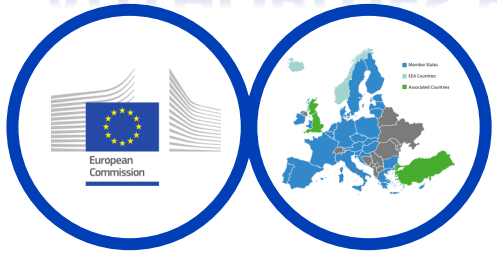
Private Members
Industry Associations

CHIPS-JU GOVERNANCE

GOVERNING BOARD



PUBLIC AUTHORITIES BOARD

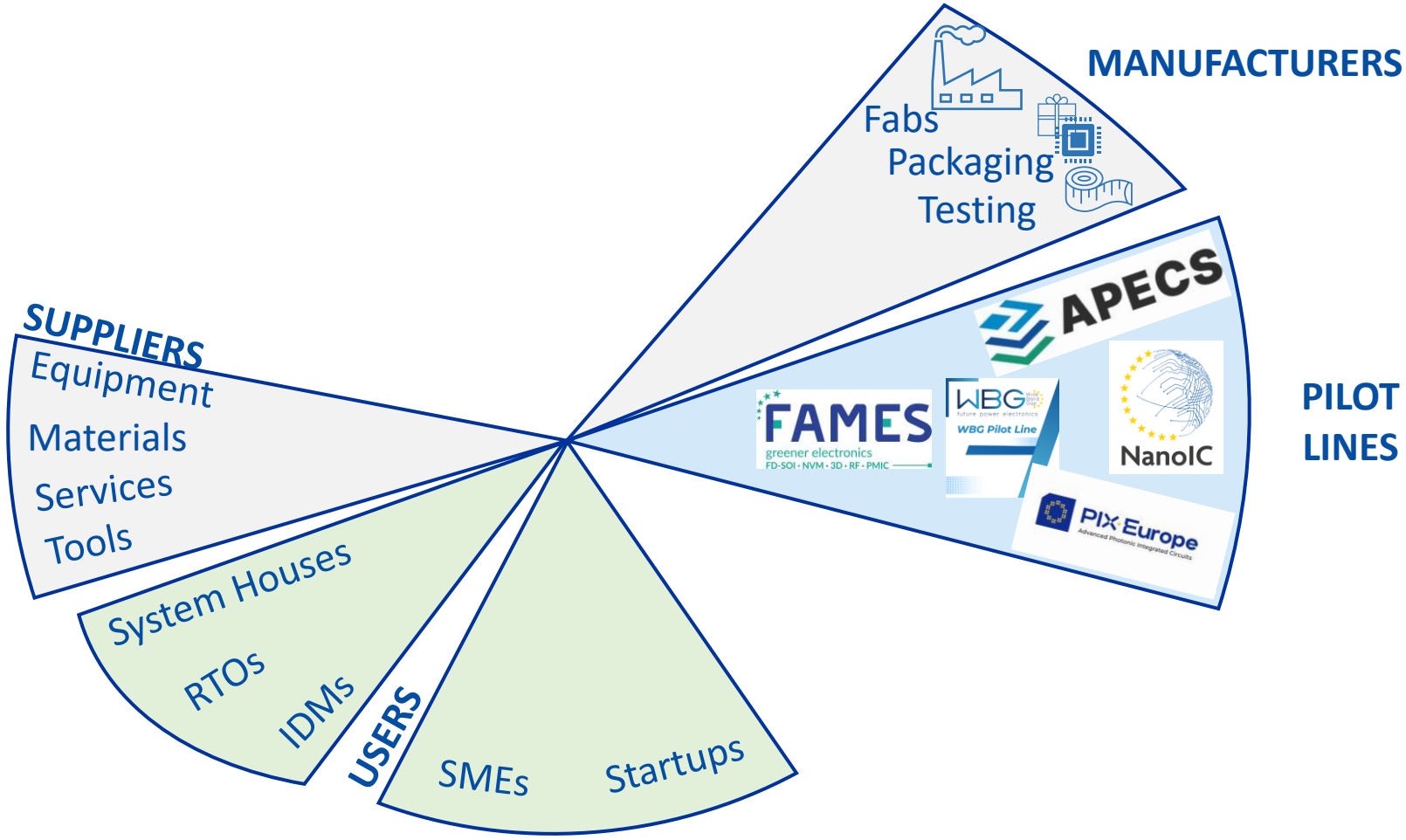


EXECUTIVE DIRECTOR

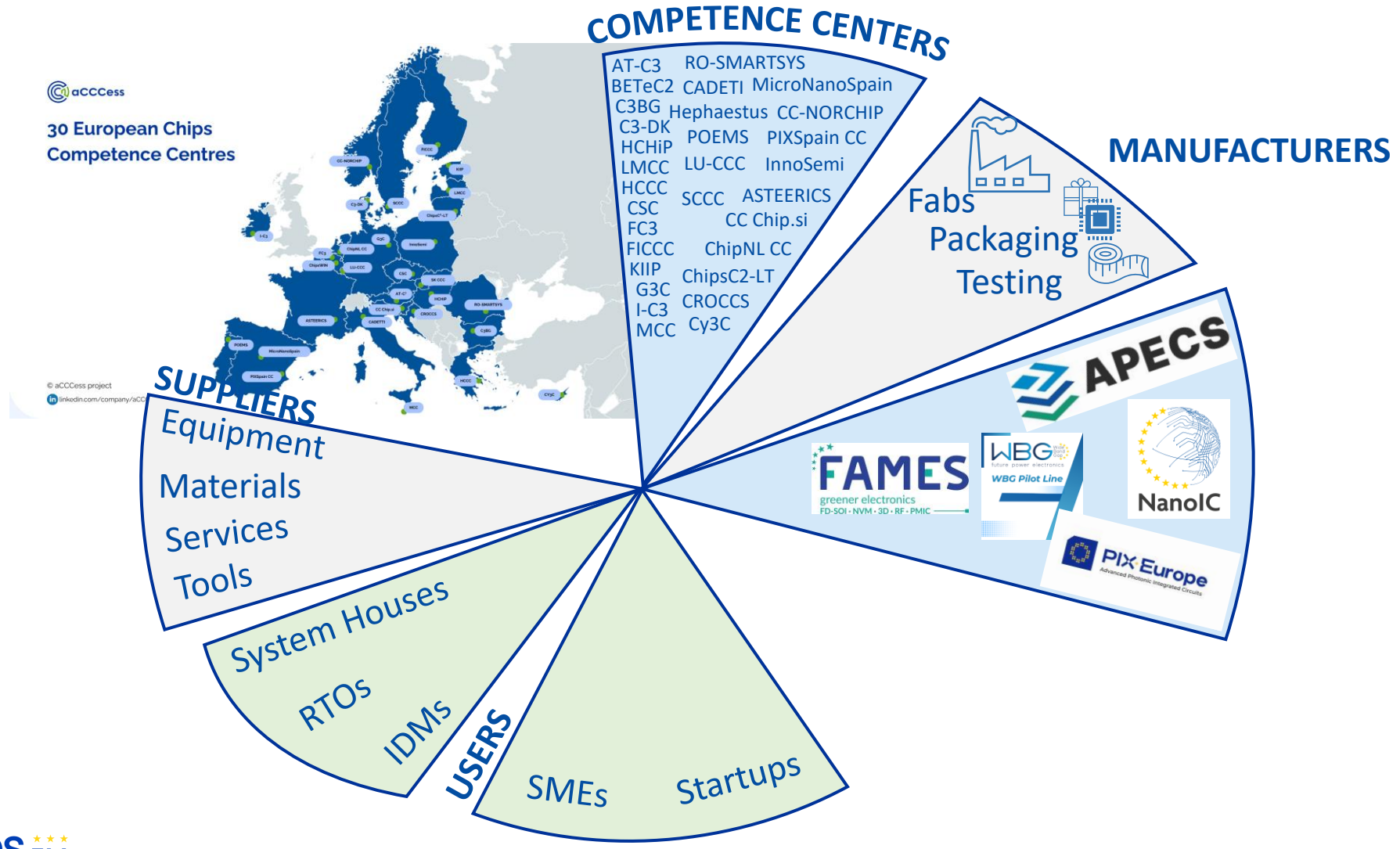
EXECUTIVE OFFICE

ELECTRONIC COMPONENTS AND SYSTEMS

CHIPS FOR EUROPE INITIATIVE PILOT LINES

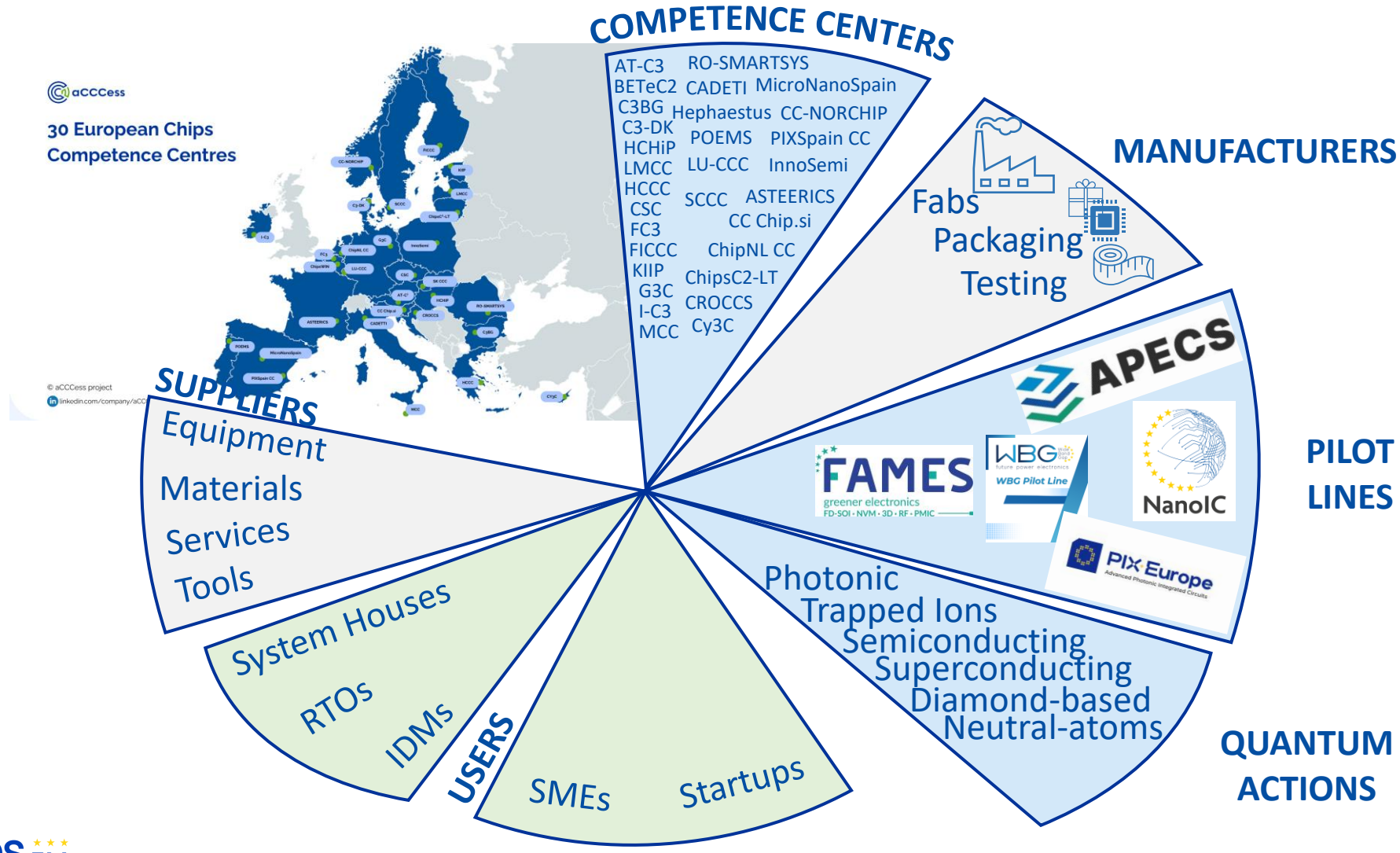


CHIPS FOR EUROPE INITIATIVE COMPETENCE CENTERS



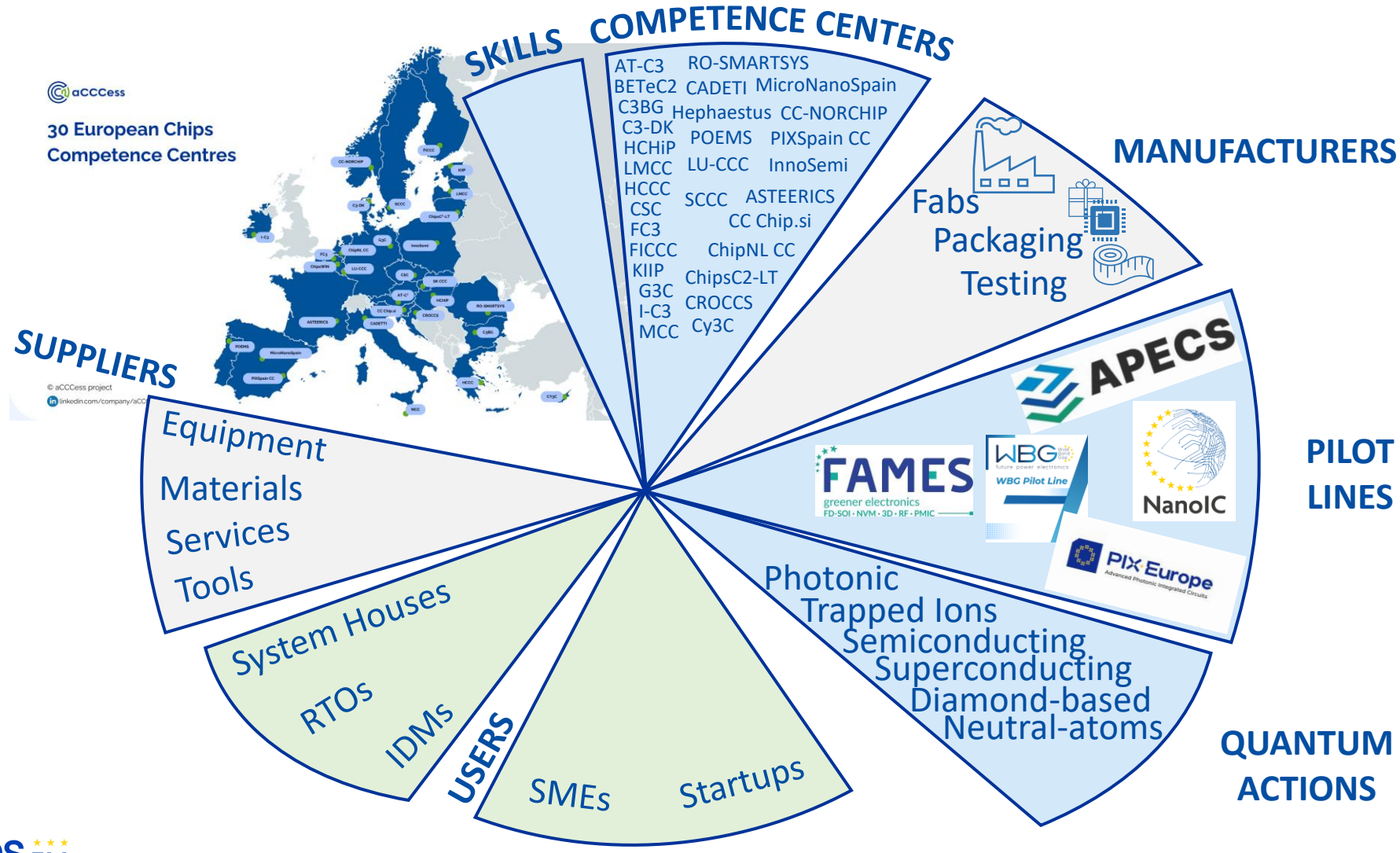
Chips JU

CHIPS FOR EUROPE INITIATIVE QUANTUM ACTIONS



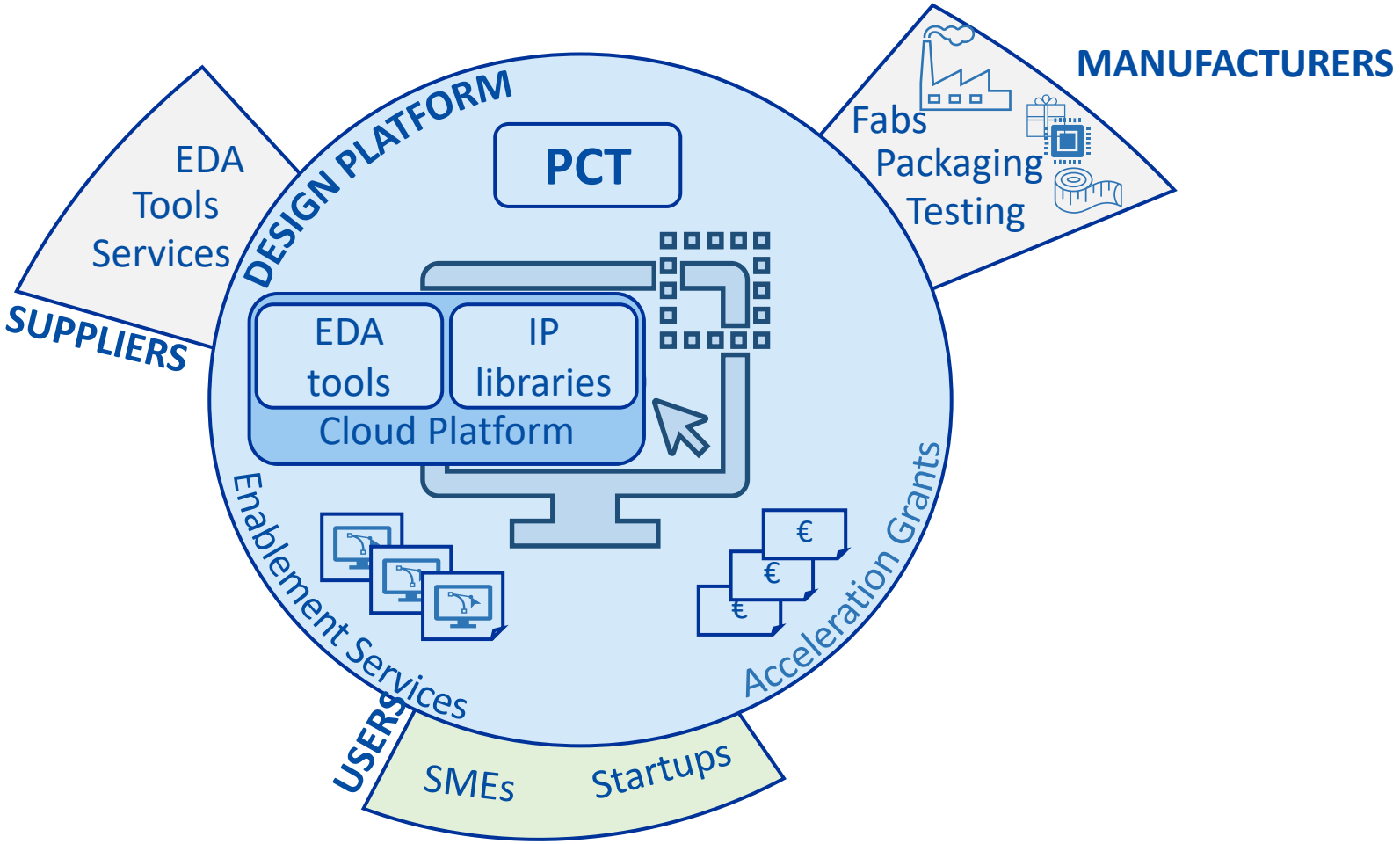
Chips JU

CHIPS FOR EUROPE INITIATIVE SKILLS

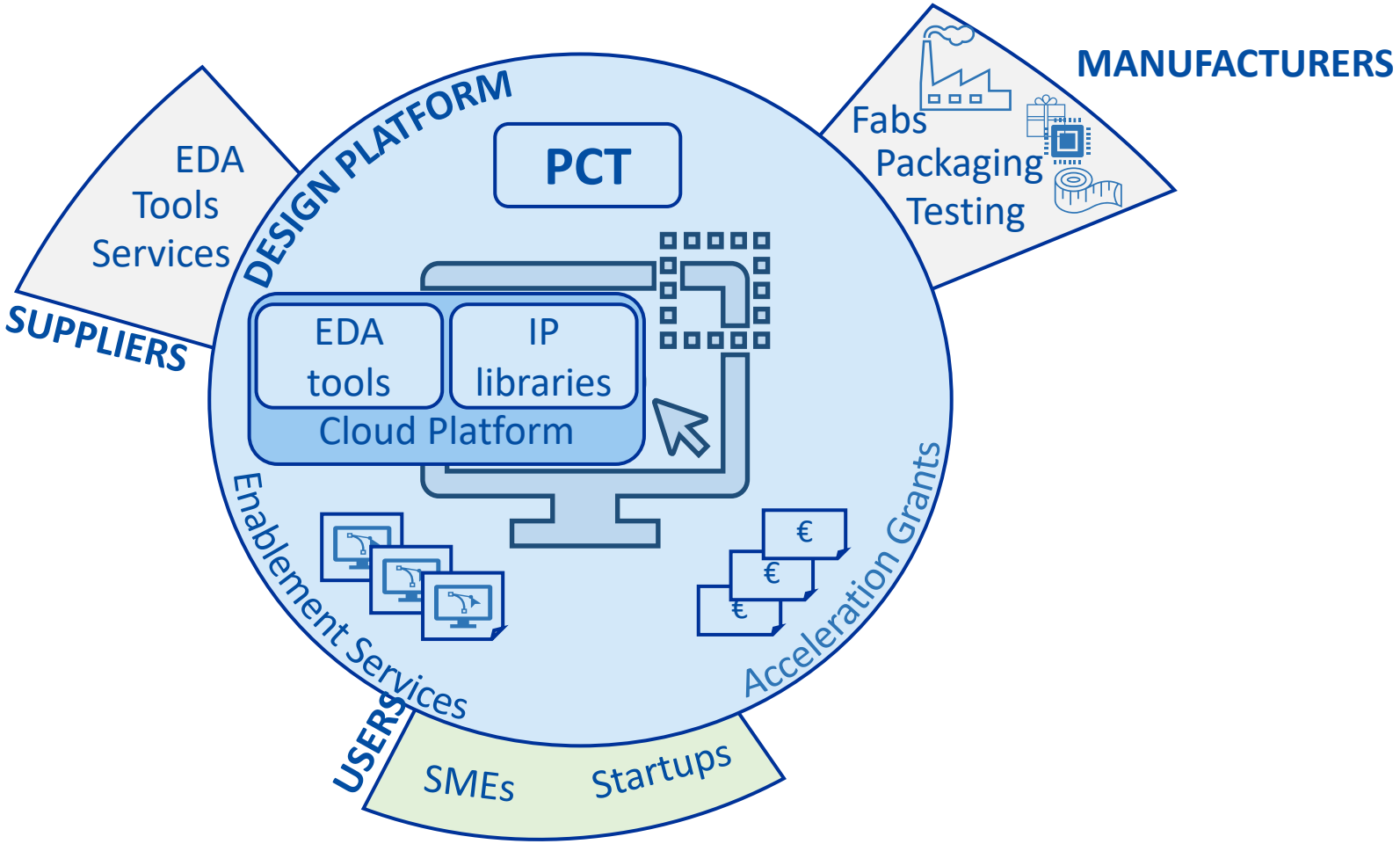


Chips JU

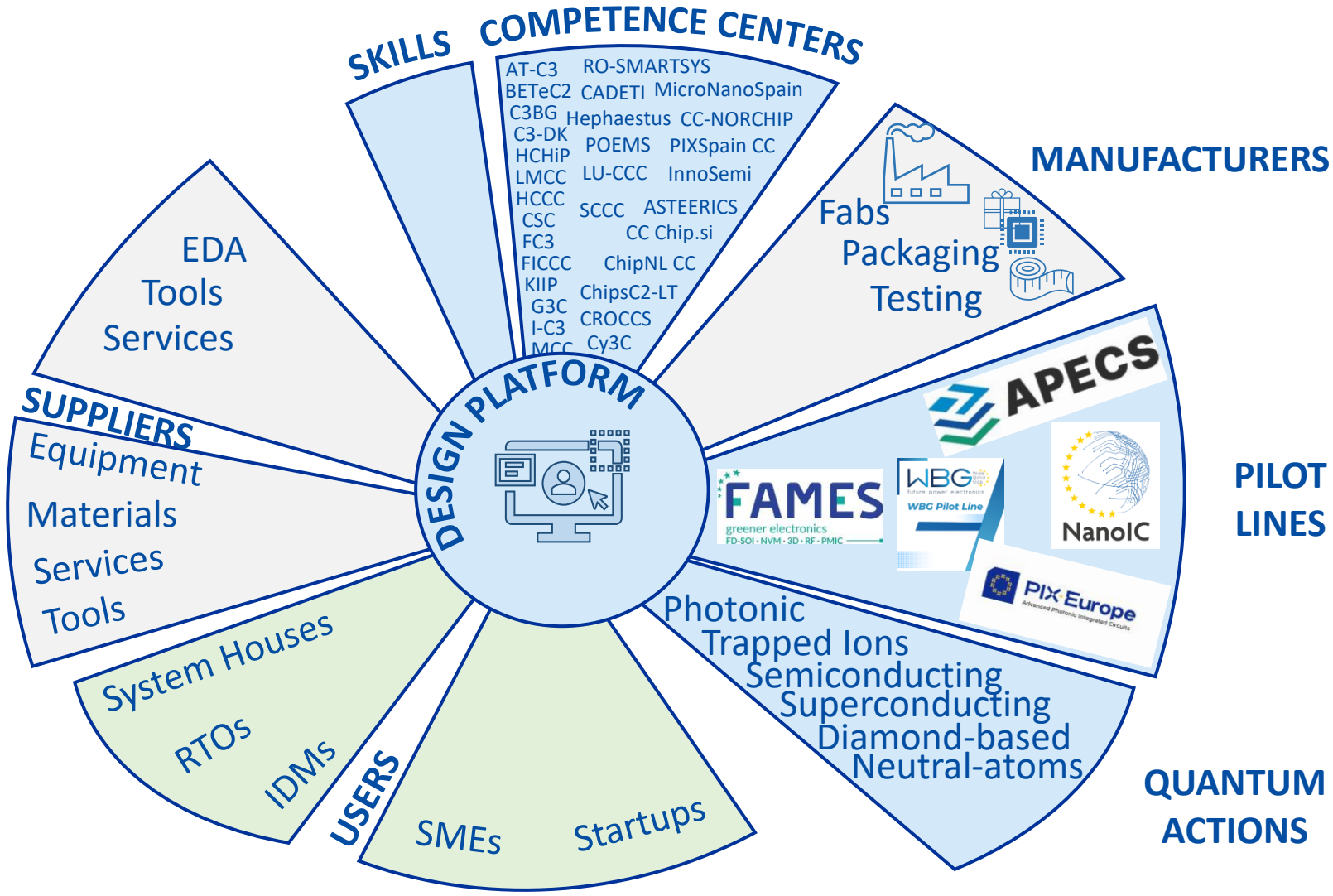
CHIPS FOR EUROPE INITIATIVE DESIGN PLATFORM



CHIPS FOR EUROPE INITIATIVE DESIGN PLATFORM

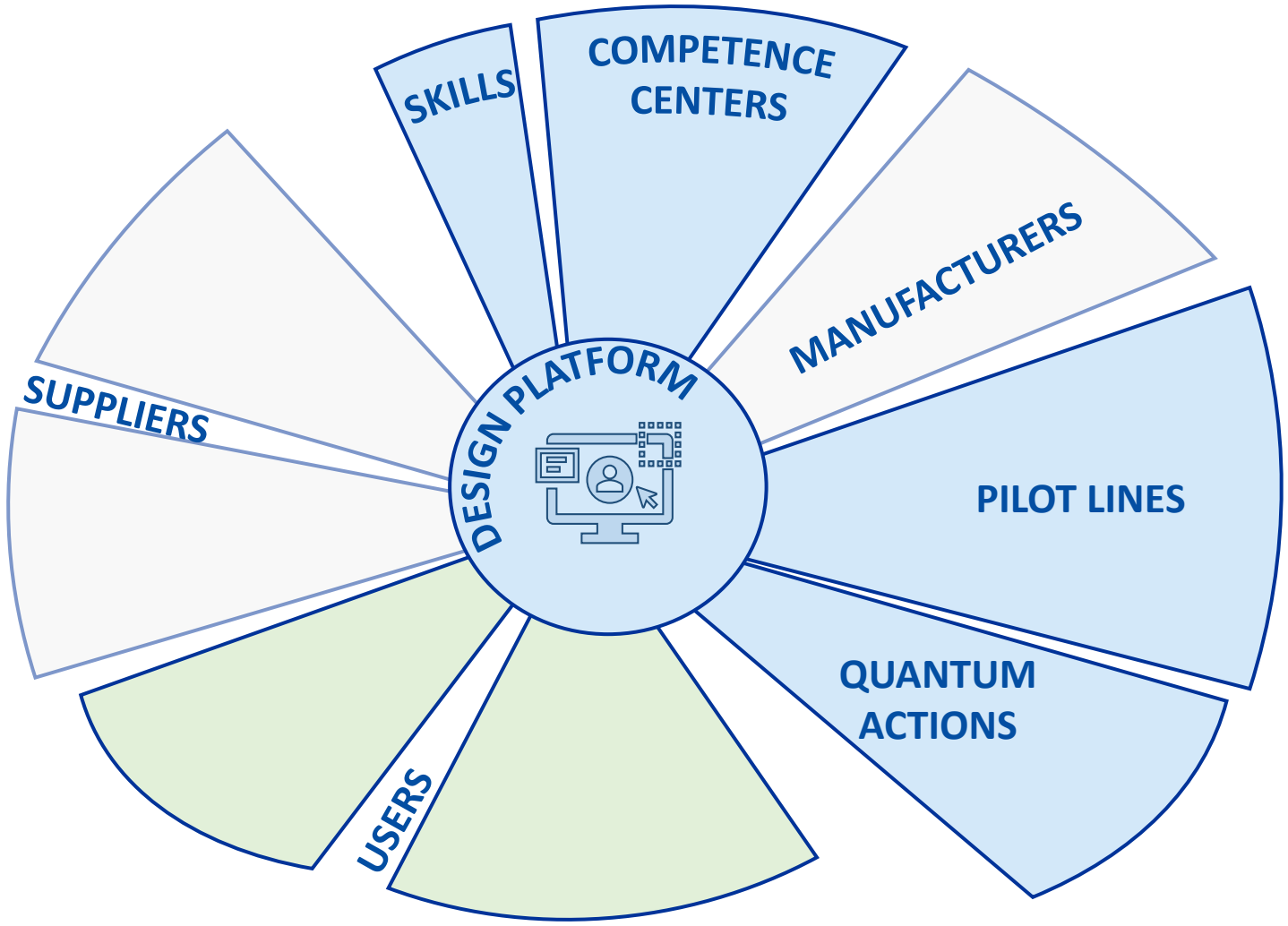


CHIPS FOR EUROPE INITIATIVE



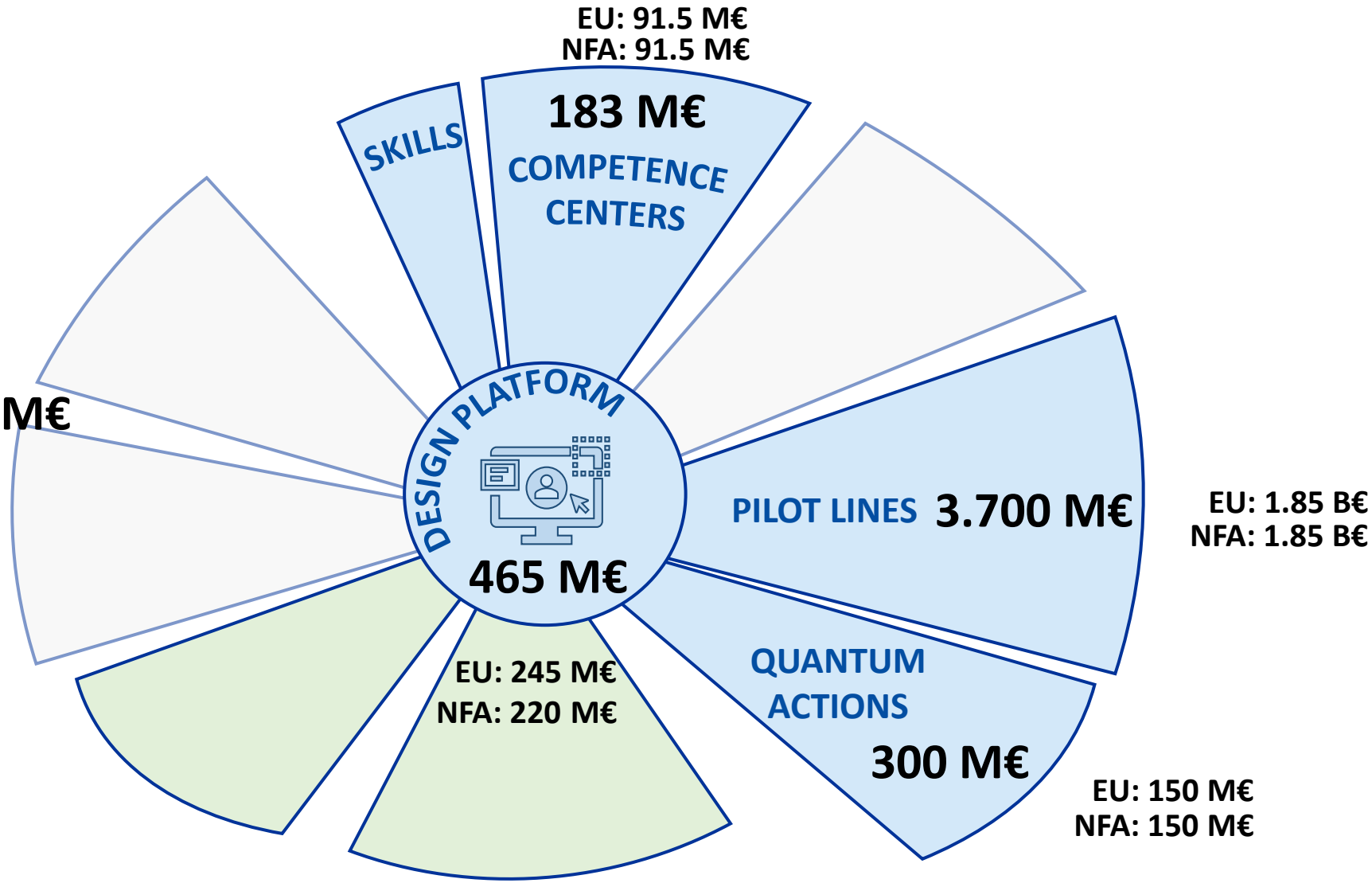
Chips JU

CHIPS FOR EUROPE INITIATIVE



CHIPS FOR EUROPE INITIATIVE

Total JU ~2.340 M€



State of Play

Chips JU

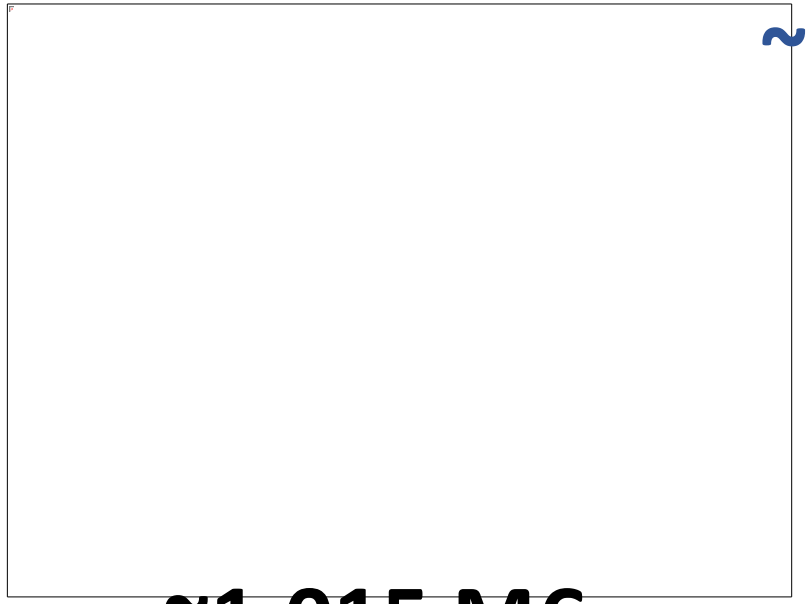
1.3 Bn

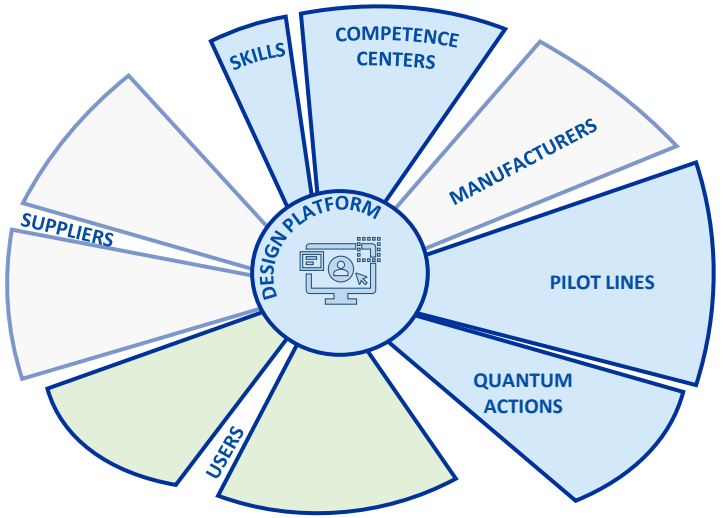
Electronic Components and Systems

~ € 4.175 Bn

2.875 Bn

Chips for Europe Initiative





~80%

~1.015 M€

~2.340 M€

Chips JU Calls 2026 Electronic Components and Systems

Anton Chichkov

10/03/2026

EU BUDGET FOR THE CHIPS JU ECS CALLS 2026

Topic	EU indicative budget (M€)
IA Global call according to SRIA 2026	40
IA Resilience call reinforcing Europe's strength in power electronics	20
IA Resilience call reinforcing Europe's strength in photonics	20
IA Resilience call reinforcing Europe's strength in health	20
AI-assisted Methods and Tools for Software-Defined Vehicle Engineering Automation	20
Global call according to SRIA 2026 (RIA)	50
RIA Resilience call reinforcing Europe's strength in 6G radio communication systems	20
Call with Digital Partnership and TTC countries	5
Supply chain resilience (CSA)	2
Coordination of the European software-defined vehicle platform	2
Total	**199**

Chips JU IA proposals

An IA proposal is characterized by:

- The activities have their centre of gravity at the **TRL 5-8.**
- Execution by **an industry led consortium**
- Developing **innovative technologies and/or using them in innovative ways**
- Establishment of a new and realistic innovation environment **connected with an industrial environment,** such as:
  - a pilot line facility capable of manufacturing
  - a zone of full-scale testing
  - a development of new processes or tools and their introduction in several domains
  - the development of frameworks or platforms together with the usage of these frameworks or platforms in innovative products.
- IA Prjects should contribute to, short to midterm **economic value creation** in Europe

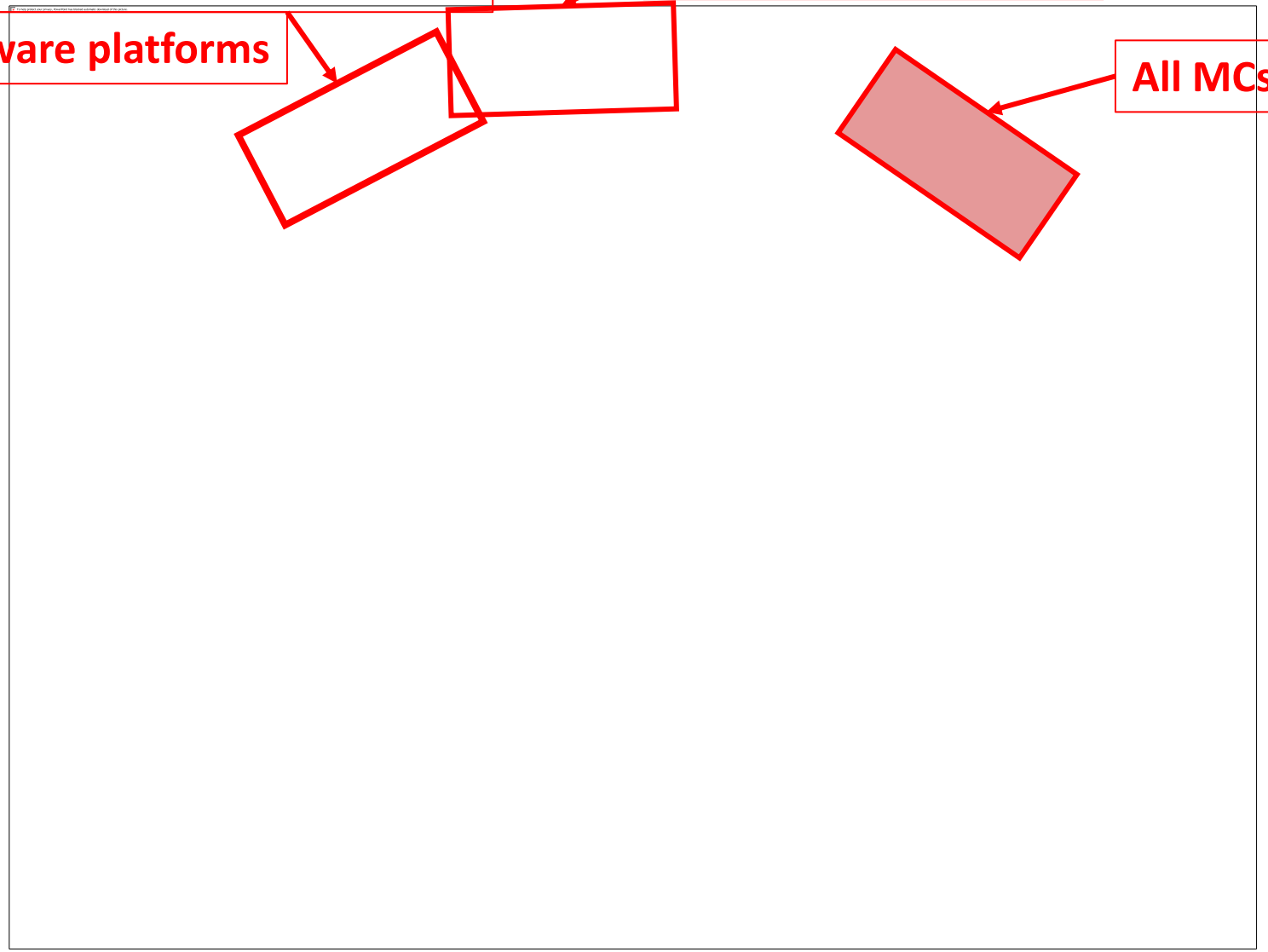
ELECTRONIC COMPONENTS AND SYSTEMS IA

MC 6: AI enabled engineering tool chain

MC 1: SDV hardware platforms

MC1:Smart & Efficient

All MCs



ELECTRONIC COMPONENTS AND SYSTEMS IA

Type of Action	Innovation Action (IA)
Indicative EU budget	40 M€
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR 15 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA Two stage Call, with submission of Project Outline (PO) and of Full Proposal (FPP)
Call launch date	03 Feb 2026
Deadline PO	07 May 2026 at 17:00 Brussels Time
Deadline FPP Stage	17 Sep 2026 at 17:00 Brussels Time

IA Resilience Call FT1
Reinforcing Europe's Strength in Power Electronics

- Cross innovations fields focusing on crucial topics should address one or more of the several domains:
  - ***WBG substrates*** to reduce EU dependency on material and provide more sustainable, industrially compatible solutions.
  - ***WBG platform*** for cost effectiveness, available in 300mm for GaN and/or SiC to improve yield and power density and close gaps in the value chain.
  - ***A toolbox*** (e.g. wafer cut, smart stacking, thin layer transfer, epitaxy, UWBG materials) for further innovation schemes.
  - Next generation or optimised **new power semiconductor devices** fitting their application.
  - **Adding *intelligence* to power** semiconductor devices on control and/or sensor side.
  - ***Facilitate*** the propagation of ***EU Packaging/Integration excellence*** along the entire value chain
  - Explore the use of heterogeneous and functional integration for ***improved performance, reliability, robustness and cost competitiveness***
  - ***Advanced characterization techniques*** for new materials, devices, and systems.
  - ***Implement AI at system level*** and/or make ***use of AI methods*** to increase the innovation speed.

Reinforcing Europe's Strength in Power Electronics

Type of Action	Innovation Action (IA)
Indicative EU budget	20 M€
Expected EU contribution per project up to:	The JU estimates that an EU contribution of around EUR 10 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call
Call launch date	7 Jul 2026
Deadline FPP Stage	17 Sep 2026 at 17:00 Brussels Time

IA Resilience FT2
Call for Reinforcing Europe's Strength in Photonics

- Proposals submitted to this call are expected to address several of the following elements:
  - **Scaling of wafer-level photonic processes** for key materials (e.g. SiN, InP, GaAs)
  - Development of **packaging and test solutions** compatible with **co-packaged optics and advanced photonic-electronic** integration.
  - **Integration of heterogeneous materials and components**, using advanced packaging and assembly approaches.
  - **Design-process-equipment co-optimisation**, enabling repeatable, cost-effective production of complex photonic circuits and systems, including use of PDKs and validated building blocks.
  - **Demonstration of system-level functionality** through application-relevant use cases in strategic sectors (e.g. AI, sensing, telecommunication, mobility, health, defence), with quantified performance metrics and clear market relevance.

Reinforcing Europe's Strength in Photonics

Type of Action	Innovation Action (IA)
Indicative EU budget	20 M€
Expected EU contribution per project up to:	The JU estimates that an EU contribution of around EUR 10 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call
Call launch date	7 Jul 2026
Deadline FPP Stage	17 Sep 2026 at 17:00 Brussels Time

IA Resilience FT3
Call for Reinforcing Europe's Strength in Health

- Proposals submitted to this call are expected to address integrated technologies for monitoring, imaging and biomedical research:
  - ***Advanced wearable health technologies and integrated solutions***
  - ***Personalized imaging technologies***
  - ***Advanced laboratory and scientific solutions***
  - Key digital technologies enabling digital healthcare transformation
  - ***Edge-to-cloud architectures*** enabling distributed data processing and decision-making across the healthcare continuum.
  - ***Embedded and edge intelligence*** for real-time analysis and adaptive system behaviour closer to the point of care.
  - ***Robust data protection frameworks*** ensuring patient privacy and compliance with healthcare regulations.
  - ***Interoperable platforms and interfaces*** to support seamless integration across devices, systems, and care settings.
  - ***AI-driven methods and tools*** for diagnostics, monitoring, prediction, and clinical decision support.
  - ***Automation and autonomous systems***, including robotics, to enhance operational efficiency and assist care delivery.

Reinforcing Europe's Strength in Health

Type of Action	Innovation Action (IA)
Indicative EU budget	20 M€
Expected EU contribution per project up to:	The JU estimates that an EU contribution of around EUR 20 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call
Call launch date	7 Jul 2026
Deadline FPP Stage	17 Sep 2026 at 17:00 Brussels Time

IA Resilience FT4
AI-assisted Methods and Tools for SDV Eng. Automation

- Proposals should particularly address the following aspects:
  - The targeted ECS-based products to be **engineered by the AI-assisted engineering solutions**
  - Adoption of **generative AI in the software engineering process**, to automate repetitive tasks
  - **AI-based engineering solutions** should be largely domain independent but shall be adopted and **showcased primarily in the software layers of the European Digital Vehicle technology stack (SDV)**.
  - **AI-assisted methods, tools and integrated platform aim at alleviating engineers' work in routine activities**
  - The dimension of **human-AI integration in the engineering process** shall improve efficiency and productivity
  - The proposed **AI-assisted methods and tools must handle multi-risk problems** in a way that are digestible by the engineers in the domain
  - The architecture **shall support service-oriented business models and model-based engineering approaches** to avoid fragmentation and unnecessary overlapping

AI-assisted Methods and Tools for SDV Eng. Automation

Type of Action	Innovation Action (IA)
Indicative EU budget	20 M€
Expected EU contribution per project	20 M€
Mode	Co-funded with the NFA One stage Call with submission of a Full Proposal (FPP)
Call launch date	03 Feb 2026
Deadline FPP stage	03 March 2026 at 17:00 Brussels Time

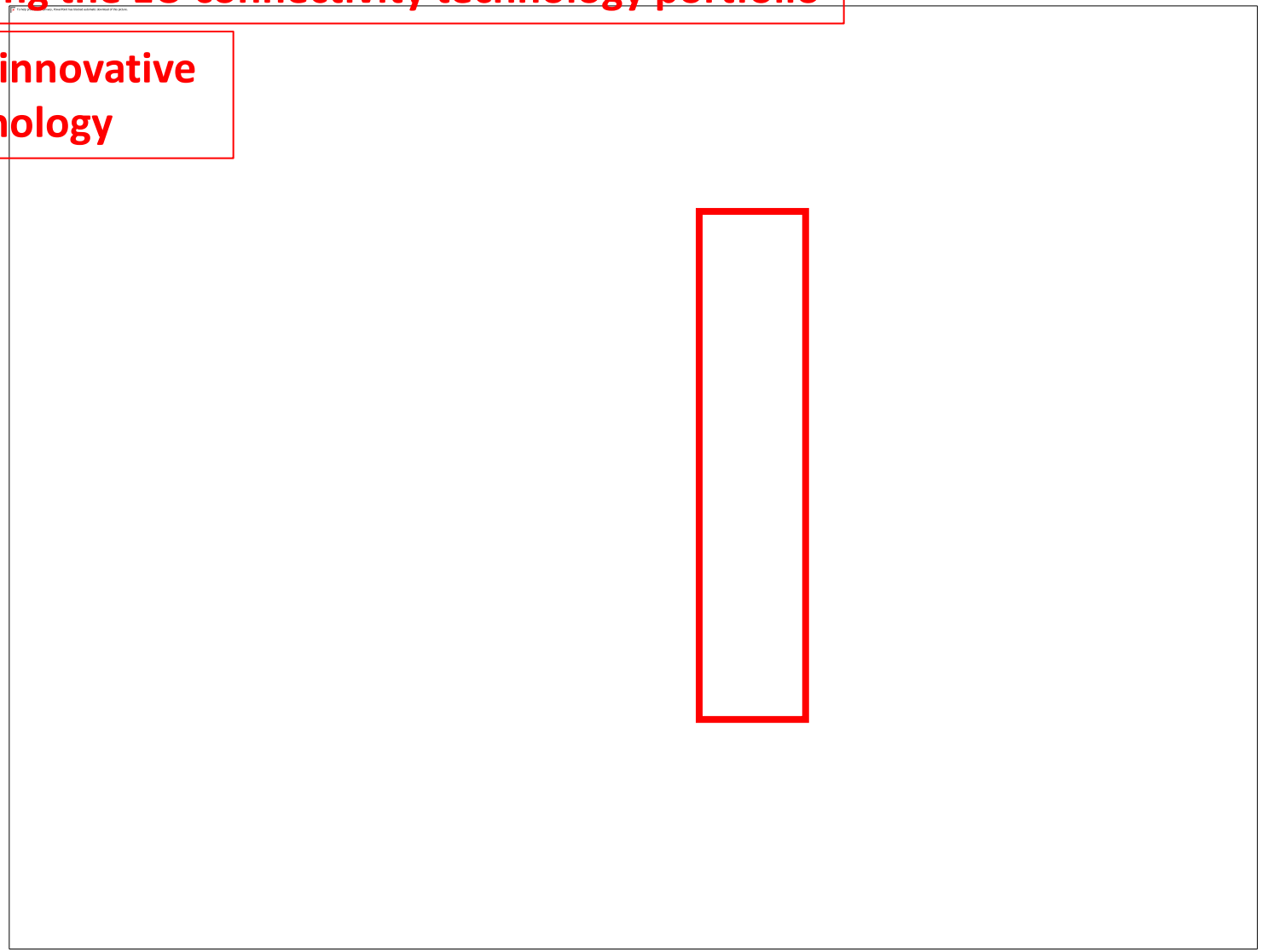
Chips JU RIA Proposals

- RIA proposal is characterized by
  - The activities have their centre of gravity at **TRL 3-4**
  - Execution normally by an **academy led consortium**
  - Developing **innovative disruptive technologies**
  - Targeting **demonstration of the innovative approach**, clearly addressing relevant societal challenges
  - Demonstrating **value and potential in a realistic lab environment** reproducing the targeted application
  - Having a **deployment plan showing the valorisation for the ECS ecosystem** and the contribution to the Chips JU goals and objectives

ELECTRONIC COMPONENTS AND SYSTEMS RIA

MC 1: Strengthening the EU connectivity technology portfolio

MC 2: Investigate innovative connectivity technology



Chips JU Global RIA

Type of Action	Research and Innovation Action (RIA)
Indicative EU budget	50 M€
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR 12 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA Two stage Call with submission of Project Outline (PO) and of Full Proposal (FPP)
Call launch date	03 Feb 2026
Deadline PO	07 May 2026 at 17:00 Brussels Time
Deadline FPP Stage	17 Sep 2026 at 17:00 Brussels Time

RIA Resilience FT1
Call on the 6G Front End Module

- Proposals submitted to this call should address the following set of FEM constituent technologies in priority including challenges issues such as:
  - **Transmitter and Power amplification**
  - **Receiver:** Very low noise and high dynamic range in receivers
  - **Filters**
  - **TRX**
  - **Integration/packaging**
  - **Sustainability:** Thermal modeling/optimization of chips modules; energy efficient designs
  - **Advanced Antenna System**
  - **ISAC:** technology for ISAC native waveforms, and showcasing practical ISAC

6G Front End Module

Type of Action	Research and Innovation Action (RIA)
Indicative EU budget	20 M€
Expected EU contribution per project up to:	The JU estimates that an EU contribution of around EUR 20 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call
Call launch date	7 Jul 2026
Deadline FPP Stage	17 Sep 2026 at 17:00 Brussels Time

ECS Int collaboration
Call with Digital Partnership and TTC countries

- The scope includes, but is not limited to, the following areas:
  - Address **research reaching TRL 4** with high potential **not yet demonstrated** in the design, fabrication process and/or packaging segments of the micro-nano-electronics and integration technologies value chain.
  - Focus **innovation on materials**, **physical concepts** or **device architecture** building on neuromorphic or integration technologies.
  - Provide a **projection of the expected gains** and **main figures of merit** of the proposed approaches.

  Multi-disciplinary research activities should address part of the semiconductor value chain from materials, processes, equipment, metrology, back-end processing to packaging, integration and tests.

ECS Int collaboration
Call with Digital Partnership and TTC countries

Type of Action	Research and Innovation Action (RIA)
Indicative EU budget	5 M€
Expected EU contribution per project	The JU estimates that an EU contribution of between EUR 2 and 2.5 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	No co-financing by Chips JU Participating States following Article 141(2) SBA One stage Call with submission of Full Proposal (FPP)
Call launch date	7 Jul 2026
Deadline FPP Stage	17 Sep 2026 at 17:00 Brussels Time

Restrictions

- Article 22(5) of the Horizon Europe Regulation shall apply to the topics in the Chips JU multiannual work programme 2023-2027 Appendix 7:

  "Activities launched in 2026 for the Electronic Components and Systems part"

  To limit participation to entities established in:

  - **EU Member States,**
  - **EEA countries,**
  - **Associated Countries,**
  - **OECD and**
  - **Mercosur countries**

ECS Supply chain resilience CSA

- The action establishes a supply chain data platform, as a digital twin of the semiconductor supply chain, which should:
  - Gather secure, anonymized data shared by companies, coming from both upstream and downstream industries.
  - Possibly make use of an existing digital reference of the semiconductor supply chain (based on semantic web technologies).
  - Be managed by a trusted intermediary and hosted on a trusted data sharing infrastructure (potentially leveraging secure Multi-Party Computation).
  - Provide access to each participating company (providing its data) to its own data and aggregate anonymised data.

ECS Supply chain resilience CSA

Type of Action	Coordination and Support Actions (CSA)
Indicative EU budget	2 M€
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR 2 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	No co-financing by Chips JU Participating States following Article 141(2) SBA One stage Call with submission of Full Proposal (FPP)
Call launch date	7 July 2026
Deadline FPP Stage	17 September 2026 at 17:00 Brussels Time

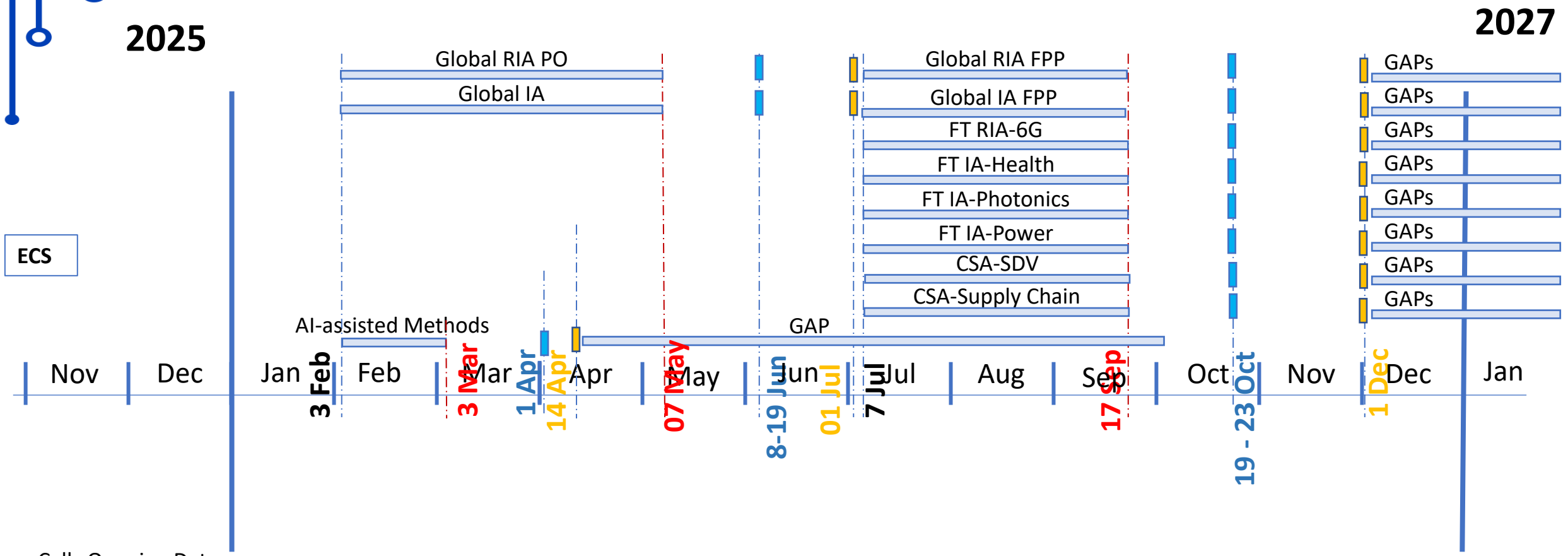
Coordination of the European SDV platform

- The action should address the following tasks:
  - Facilitate regular updates of the joint technical roadmap for a common open SDV platform, created under the coordination of FEDERATE, with gradual roll out and aiming for the start of full operation as soon as possible, but at latest in 2030;
  - Facilitate the development and agreement on an open reference architecture for the software-defined vehicle;
  - Support the Commission and the Chips JU in maintaining a high-level governance structure for research and innovation actions under the Chips JU, and beyond, targeting the vehicle of the future.
  - Support and cooperate with the Chips JU in structuring, steering and coordinating the Focus Area, notably by integrating the outcomes of the different actions in its roadmap and reference architecture, by ensuring the coherence of these actions with the overall governance of the initiative and by contributing to establishing a framework for the sustainability, maintenance and continuous development of the actions' outcomes;
  - Ensure regular exchange, alignment, and a common holistic roadmap with other activities under the Chips Act, focusing on EU-designed open-source hardware for the automotive sector;
  - Follow and align with related Member States projects, other EU funding instruments and partnerships (e.g. CCAM, 2ZERO) and support the development of an EU-wide investment roadmap;
  - Positioning vis-à-vis automotive initiatives such as AUTOSAR, COVESA, the ECLIPSE Foundation SDV Working Group, SOAFEE, Catena-X, etc. and SDV-related developments in other global regions;
  - Steer consensus on jointly developed open source components of the SDV software stack, drawing from the outcomes of the projects in the Focus Area, and coordinating with related initiatives to support convergence;
  - Facilitate the establishment of a sustainable framework for an open European SDV platform and ecosystem;
  - Organise a European conference on automotive software, targeting software engineers and developers, building on the open-source projects stemming actions under the Focus Area and related initiatives, in partnership with leading European industrial players.

Coordination of the European SDV platform

Type of Action	Coordination and Support Action (CSA)
Indicative EU budget	2 M€
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR 2 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	EU funding only One stage Call with submission of Full Proposal (FPP)
Call launch date	07 Jul 2026
Deadline FPP Phase	17 Sep 2026 at 17:00 Brussels Time

PLANNING CHIPS-JU ECS CALLS 2026



Calls Opening Date
Calls Deadline
Proposals Evaluation
PAB Dec
PAB Amended Funding Dec

EUROPEAN PARTNERSHIP

Chips JU Calls 2026
Chips for Europe Initiative

Anton Chichkov

10/03/2026

Chips for Europe Initiative

- HE Actions

Description	Indicative EU budget M€
Quantum Chips Design: Driving Europe's Quantum Design Ecosystem and Enabling Quantum Design Tools Innovation	**30**
Quantum Chips: Enabling Technologies	**20**
Total	**50**

Chips for Europe Initiative

- DEP Actions

Description	Indicative EU budget M€
Call for Design Enablement Teams	**5**
Skills Hubs of Excellence	**20**
Pilot Federation	**10**
Stimulation of Chip Design	**15**
International collaboration - Joint call EU and Japan on semiconductors	**15**
AI chips and systems for EU compute infrastructure	**100**
Total	**165**

Skills: Pilot Federation

- Projects funded under this call establishing the ‘Pilot Federation’ should network European VET providers with focus on vocational training.
- Projects should deliver several of the following elements:
  - Provide a **comprehensive overview of the micro-credential offer** and the **relevant providers** in the semiconductor sector in Europe.
  - Develop a **pilot scalable network of VET providers** and an industry-aligned micro-credentials ecosystem in Europe for the semiconductor sector.
  - Design **training programmes through partnerships among VET providers** and business to **align courses more closely with industry needs** with **focus on reskilling** programmes for professionals transitioning from other industrial sectors experiencing surplus workforce.
  - Place **emphasis on micro-credentials**, a flexible tool for rapid upskilling and lifelong learning.
  - **Encourage cross-border collaboration**.
  - **Attract extra-EU migration** of workers

Skills: Pilot Federation

Type of Action	Simple Grant
Indicative EU budget	**10 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR **10 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

Skills: Stimulation of Chip Design

- **Organising and implementing a comprehensive Chip Design Skills Programme** aimed at inspiring new generations to pursue careers in the semiconductor sector.
- **For students at both higher education** institutions in relevant disciplines **and secondary schools**.
- To be **developed as part of a broader continuum of European semiconductor skills initiatives**, ensuring strong complementarities and synergies with existing efforts such as **EUROPRACTICE** and the **Design Platform** and **Competence Centres**.
- Activities should be **widely disseminated** and **accessible** to relevant parties **in all EU 27 Member States**.

Skills: Stimulation of Chip Design

Type of Action	Coordination and Support Action (**CSA**)
Indicative EU budget	**15 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around **EUR 15 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	EU funding only One stage Call with submission of Full Proposal (FPP)]
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

Skills Hubs of Excellence

The text in this subsection should be seen as a placeholder.
The exact manner in which the funding will be allocated will be defined in a later stage.

Type of Action	Simple Grant
Indicative EU budget	**20 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR **10 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

Quantum Chips Design: Driving Europe's Quantum Design Ecosystem and Enabling Quantum Design Tools Innovation

- **Foster a pan-European community around quantum chip design**.
- **Research, development, and validation of European quantum design tools**, covering chip design, layout, simulation, verification, and flow integration, including Process Design Kit (PDK) interface coding, software layers, APIs, and data.
- **Effective progression from community alignment to operational deployment**
- **Establishing formal interfaces and operating procedures with relevant Chips JU pilot lines** (including quantum-focused Quantum Pilots) and European pilot lines in microelectronics and photonics.
- The action should **ensure interoperability across platforms**, reduce duplication of effort, and **establish a sustainable repository of fully verified and validated design libraries**.
- **Connect design with fabrication**, to support quantum-compatible fabrication access.
- Proposals should document **concrete access arrangements to at least one relevant pilot line/foundry** and demonstrate **alignment with the European Design Platform** onboarding process.

Chips JU

Quantum Chips Design: Driving Europe's Quantum Design Ecosystem and Enabling Quantum Design Tools Innovation

Type of Action	Research and Innovation Action (**RIA**)
Indicative EU budget	**30 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around **EUR 30 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

Quantum Chips: Enabling Technologies

- This topic focuses on enabling technologies that support, control, and read out quantum systems without funding the core quantum chips themselves
- Proposals should target **system-level integration and interfaces**. Solutions may include for example:
  - **Control and readout electronics** across temperature stages including cryogenic
  - **Photonic/optical components** for routing, modulation, detection and timing
  - **Transduction and networking technologies** such as microwave-optical conversion
  - **Cryogenics, interconnects, packaging and heterogeneous integration** for modular assemblies
- The topic **covers two complementary categories of enabling technologies**:
  - Process Enabling Technologies
  - Operations Enabling Technologies.
- This topic **does not fund the manufacturing of core quantum chips/QPUs**.

Quantum Chips: Enabling Technologies

Type of Action	Research and Innovation Action (**RIA**)
Indicative EU budget	**20 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around **EUR 5 to 7 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	**Co-funded with the NFA** One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

International collaboration - Joint call EU and Japan on Semiconductors

- The scope includes, but is not limited to, the following areas:
  - Develop **methods for chiplet co-optimization**, **interface design**, and **2.5D/3D integration** processes, including through-silicon vias, interposers, and bonding techniques.
  - **R&I on advanced fabrication processes**.
  - Engage material scientists, chemical engineers, semiconductor manufacturers, and AI experts to bridge research and industrial applications, supporting broad adoption and commercial viability.

Proposals should **encourage partnerships across industry, academia, and research organizations** to foster breakthroughs in semiconductor manufacturing and contribute to advancing global semiconductor standards.

International collaboration - Joint call EU and Japan on Semiconductors

The text in this subsection should be seen as a placeholder.
The exact manner in which the funding will be allocated will be defined in a later stage.

Type of Action	Simple Grant (**SG**)
Indicative EU budget	**15 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around **EUR 5 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	**Co-funded with the NFA** One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Stage	*17 Sep 2026 at 17:00 Brussels Time*

Call for Design Enablement Teams

- Each **DET is in charge managing a distributed cloud instance** and **providing dedicated application engineering support** to users from setting up their design environment and design flows up to tape-out.
- A **DET can be a single entity**, **or a consortium** of entities selected among providers of chips design support services, such as design houses, RTOs or other entities currently providing design enablement services on a commercial basis.
- **DETs should be selected based on their technology expertise**, ability to offer support across the end-to-end design flow, **access to fabrication services** (foundries, packaging, test services) and a **proven track record** of delivering high quality services to users, amongst other characteristics.

Call for Design Enablement Teams

The text in this subsection should be seen as a placeholder.
The need for additional DET will be defined in a later stage.

Type of Action	Coordination and Support Action (CSA)
Indicative EU budget	**5 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around **EUR 0.5 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	**EU funding only** One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

AI chips and systems for EU compute infrastructure

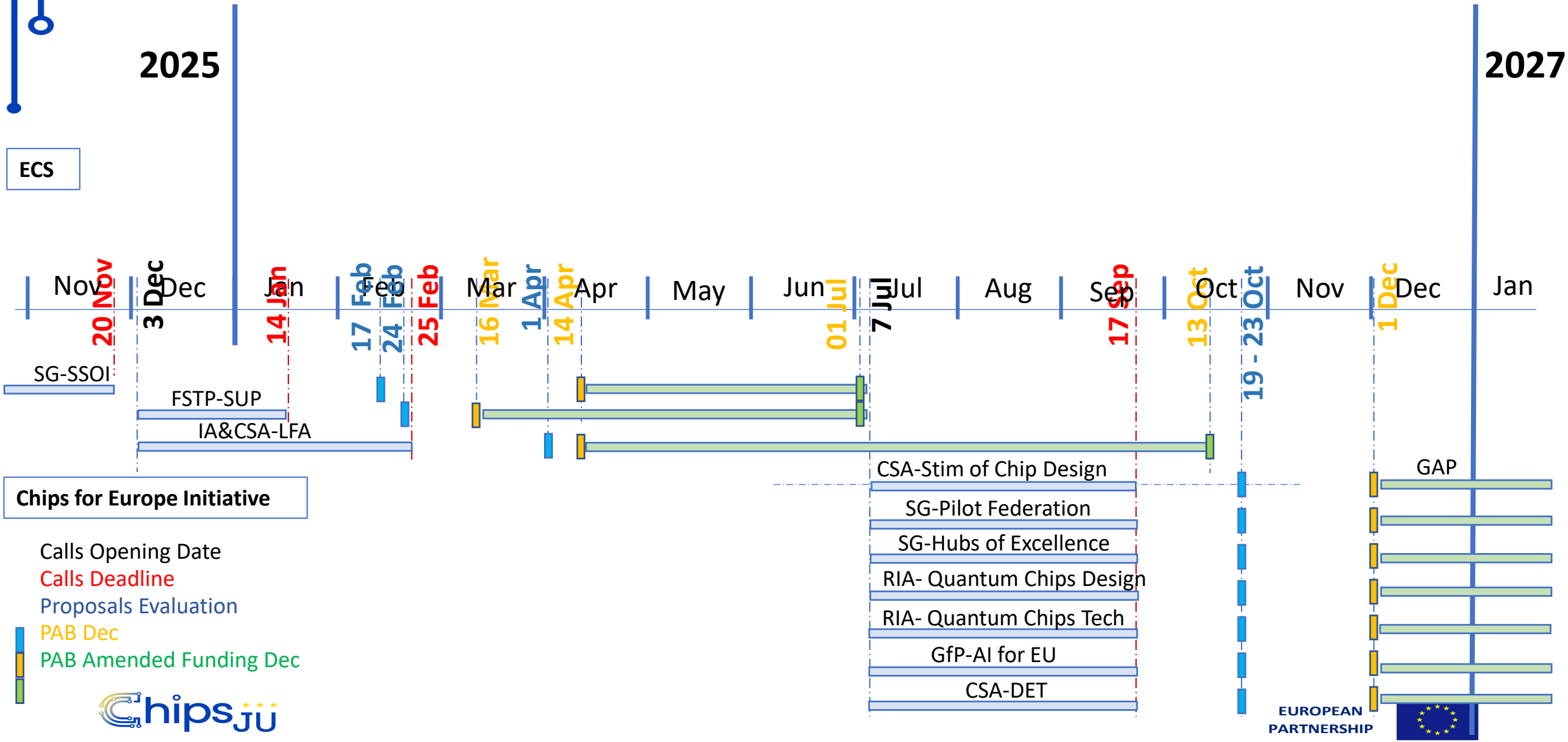
- Proposals submitted to this call are expected to address the following elements:
  - The consortium will form a buyers' group of procurers under EU law, that will set up and run a Pre-Commercial Procurement (PCP) in staged phases, ensuring competition to the end.

AI chips and systems for EU compute infrastructure

The text in this subsection should be seen as a placeholder.
The exact manner in which the funding will be allocated will be defined in a later stage.

Type of Action	Grant for Procurement
Indicative EU budget	**100 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of **EUR 100 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	**Co-funded with the NFA** One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

PLANNING CHIPS-JU ECS CALLS 2026



CHIPS FOR EUROPE INITIATIVE CALLS AND ACTIONS

Topic	Programme	Type of action	NFA Co-funding	Budget M€	Max Per Proposal M€
Design Platform - DET	DEP	CSA	NO	5	0.5
Design Platform - AI chips and systems for EU compute infrastructure	DEP	GfP	YES	100	100
Skills - Hubs of Excellence	DEP	SG	YES	20	
Skills - Pilot Federatin	DEP	SG	YES	10	
Skills - Stimulation of Chip Design	DEP	CSA	YES	15	
Quantum-- Chps Design	HE	RIA	YES	30	
Quantum - Enabling Tech	HE	RIA	YES	20	
INCO with Japan	DEP	SG	YES	15	
				215	

Topic	Programme	Dates		Funding %			Restirictions
		Open	FPP	LE	SME	Other	
Design Platform - DET	DEP	7/7/2026	17/09/2026	100%	100%	100%	MS, Iceland and Norway
Design Platform - AI chips and systems for EU compute infrastructure	DEP	3/2/2026	12/5/2026	50%	50%	50%	MS, Iceland and Norway
Skills - Hubs of Excellence	DEP	7/7/2026	17/09/2026	50%	50%	50%	MS, Iceland and Norway
Skills - Pilot Federatin	DEP	7/7/2026	17/09/2026	50%	50%	50%	MS, Iceland and Norway
Skills - Stimulation of Chip Design	DEP	7/7/2026	17/09/2026	50%	50%	50%	DEP
Quantum-- Chps Design	HE	7/7/2026	17/09/2026	50%	50%	50%	MS, Iceland and Norway, CA, IL, KR, NZ, CH and UK
Quantum - Enabling Tech	HE	7/7/2026	17/09/2026	50%	50%	50%	MS, Iceland and Norway, CA, IL, KR, NZ, CH and UK
INCO with Japan	DEP	7/7/2026	17/09/2026	50%	50%	50%	MS, Iceland and Norway